FIG. 1
CONVENTIONAL ART

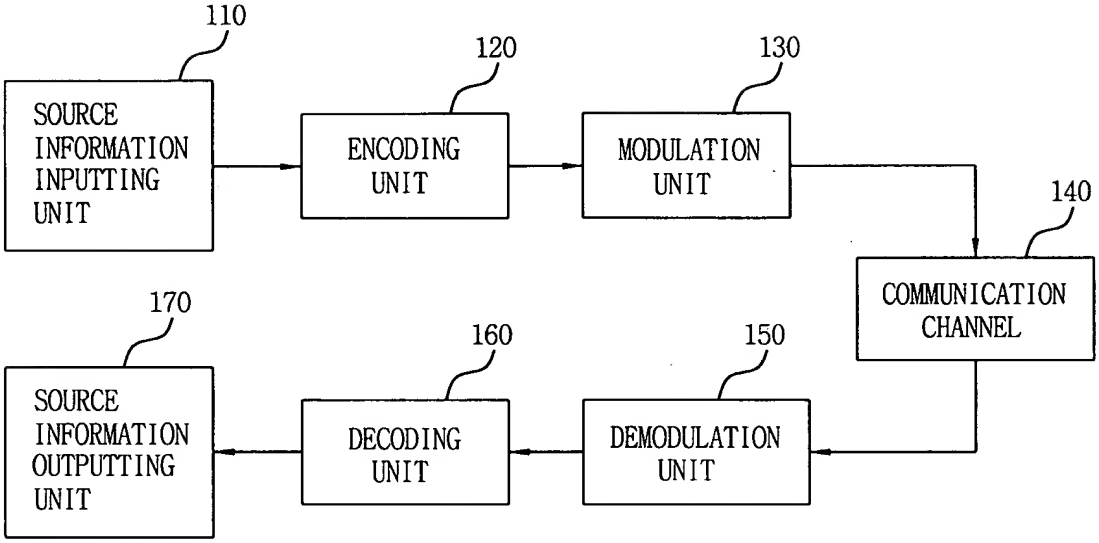

FIG. 2
CONVENTIONAL ART

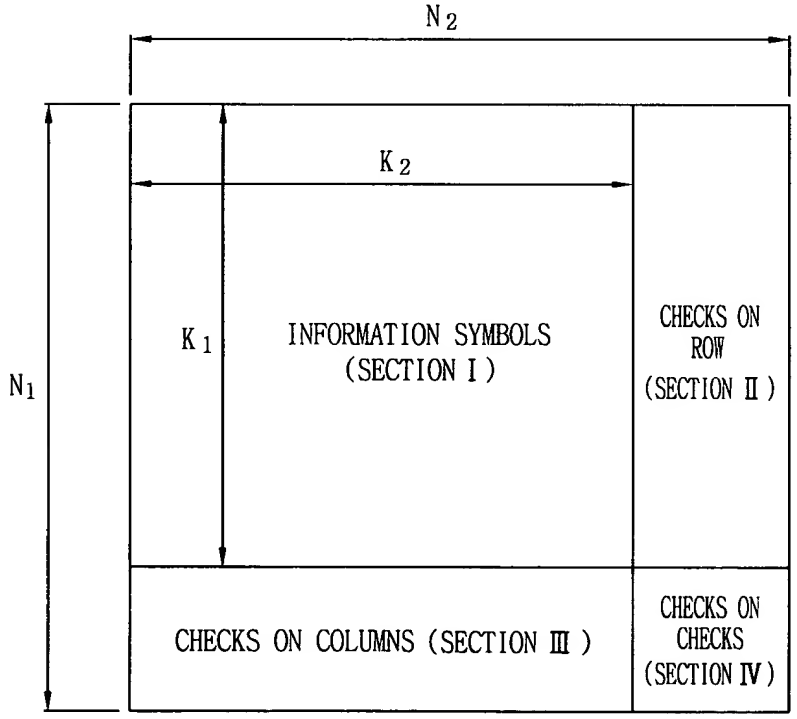

FIG. 3

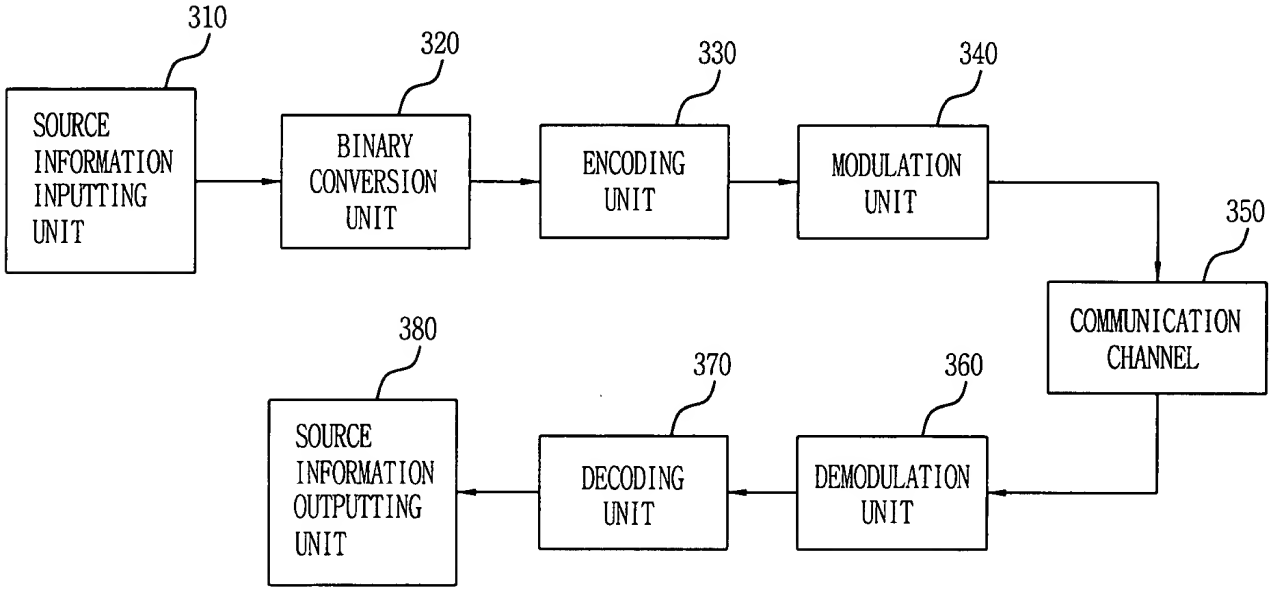
310
SOURCE INFORMATION INPUTTING UNIT
320
BINARY CONVERSION UNIT
330
ENCODING UNIT
340
MODULATION UNIT
350
COMMUNICATION CHANNEL
360
DEMODULATION UNIT
370
DECODING UNIT
380
SOURCE INFORMATION OUTPUTTING UNIT

FIG. 4

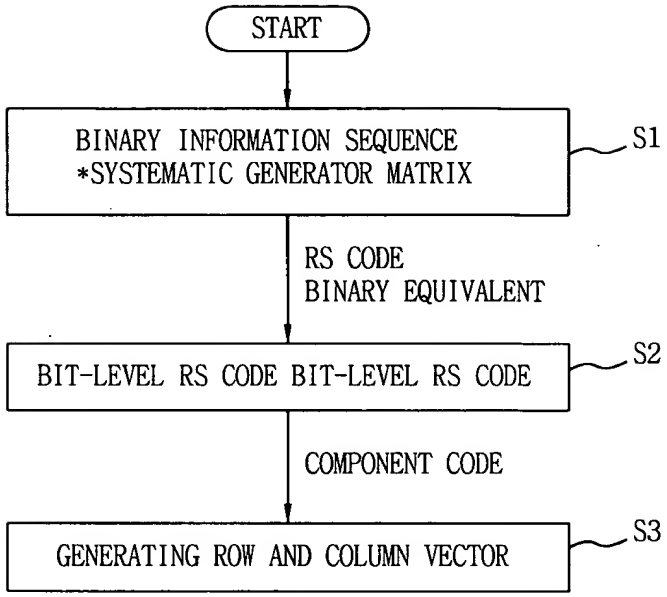

FIG. 5

$$G_b = \begin{vmatrix} \begin{bmatrix} \alpha^{m-1} & g_{00} \\ \vdots & \\ \alpha^{0} & g_{00} \end{bmatrix} & \cdots\cdots\cdots & \begin{bmatrix} \alpha^{m-1} & g_{0N-1} \\ \vdots & \\ \alpha^{0} & g_{0N-1} \end{bmatrix} \\ \vdots & \cdots\cdots\cdots & \vdots \\ \begin{bmatrix} \alpha^{m-1} & g_{k-1,0} \\ \vdots & \\ \alpha^{0} & g_{k-1,0} \end{bmatrix} & \cdots\cdots\cdots & \begin{bmatrix} \alpha^{m-1} & g_{K-IN-1} \\ \vdots & \\ \alpha^{0} & g_{K-IN-1} \end{bmatrix} \end{vmatrix}$$

FIG. 6

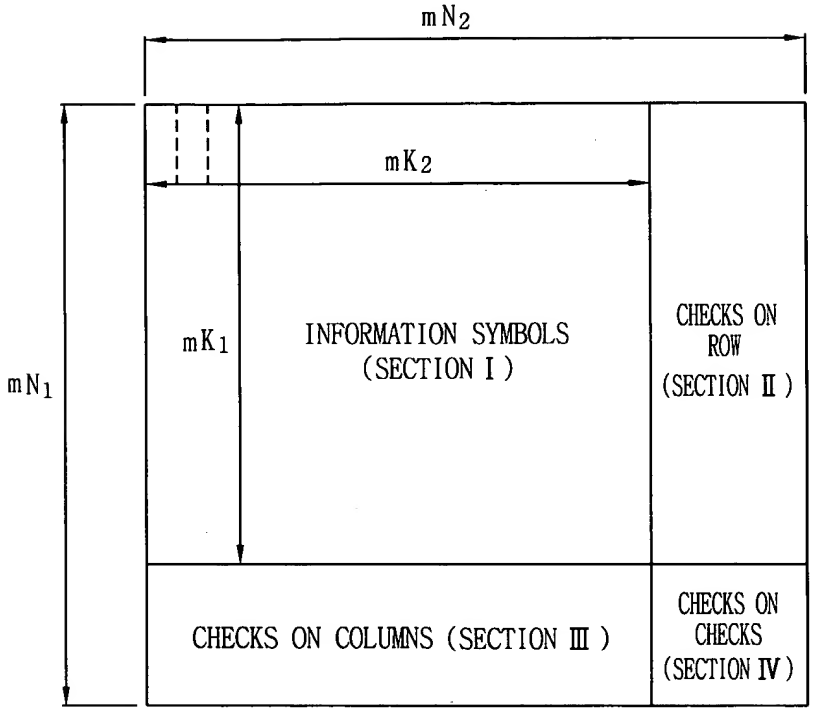
mN2
mK2
mK1
mN1
INFORMATION SYMBOLS
(SECTION I)
CHECKS ON
ROW
(SECTION II)
CHECKS ON COLUMNS (SECTION III)
CHECKS ON
CHECKS
(SECTION IV)

FIG. 7

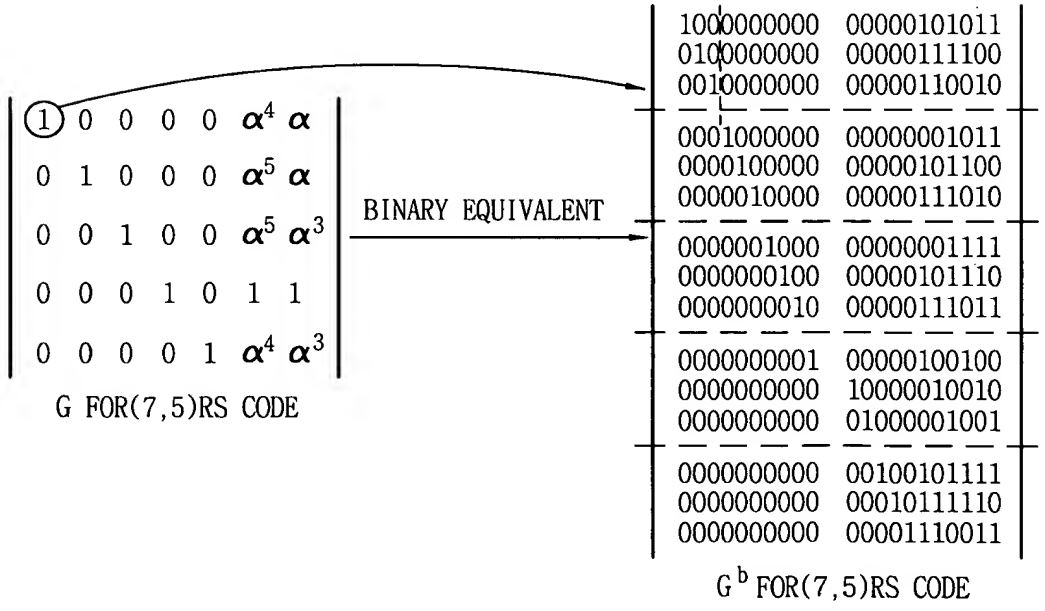
1 0 0 0 0 α4 α
0 1 0 0 0 α5 α
0 0 1 0 0 α5 α3
0 0 0 1 0 1 1
0 0 0 0 1 α4 α3
G FOR(7,5)RS CODE
BINARY EQUIVALENT
1000000000 00000101011
0100000000 00000111100
0010000000 00000110010
0001000000 00000001011
0000100000 00000101100
0000010000 00000111010
0000001000 00000001111
0000000100 00000101110
0000000010 00000111011
0000000001 00000100100
0000000000 10000010010
0000000000 01000001001
0000000000 00100101111
0000000000 00010111110
0000000000 00001110011
G b FOR(7,5)RS CODE

FIG. 8